

**We Claim:**

- 1           1.       A method of forming a silicon dioxide layer, comprising:  
2           providing a semiconductor substrate, the semiconductor substrate having at least  
3           one silicon surface region having a curved surface;  
4           roughening the surface of the at least one silicon surface region to produce a layer  
5           of porous silicon, roughening the surface of the at least one silicon surface region includes  
6           forming pores, the pores each having a width of less than 20 nm and a pore depth of less  
7           than 20 nm;  
8           thermally oxidizing the at least one roughened curved silicon surface region; and  
9           oxidizing the at least one silicon surface region to produce an oxidized portion  
10          within the semiconductor substrate which ends at a depth, the depth being greater than the  
11          pore depth of the pores.
- 1           2.       The method of claim 1, wherein roughening the surface of the at least one  
2           silicon surface region includes producing pores, the pores each having a size of less than  
3           10 nm.
- 1           3.       The method of claim 2, wherein roughening the surface of the at least one  
2           silicon surface region includes producing pores, the pores each having a size of less than 5  
3           nm.
- 1           4.       The method of claim 1, wherein roughening the surface of the at least one  
2           silicon surface region includes etching the surface region.

1           5.       The method of claim 4, wherein etching the surface region includes etching  
2   in a solution containing phosphoric acid.

1           6.       The method of claim 4, wherein etching the surface region includes etching  
2   in a solution including  $\text{H}_2\text{SO}_4$ , HF and  $\text{HNO}_3$ .

1           7.       The method of claim 6, wherein etching the surface region includes etching  
2   in a solution having a composition of  $\text{H}_2\text{SO}_4:\text{HF}:\text{HNO}_3 = 7:1:0.01$ .

1           8.       The method of claim 4, wherein roughening the surface of the at least one  
2   silicon surface region includes electrochemically etching the surface region.

1           9.       The method of claim 8, wherein roughening the surface of the at least one  
2   silicon surface region includes etching the surface region with a mixture of hydrofluoric  
3   acid and ethyl alcohol.

1           10.      The method of claim 9, wherein roughening the surface of the at least one  
2   silicon surface region includes etching the surface region with a mixture of 49% aqueous  
3   hydrofluoric acid and pure ethyl alcohol at a ratio of 0.75:0.25.

1           11.      The method of claim 8, wherein roughening the surface of the at least one  
2   silicon surface region includes etching the surface region with a 6% aqueous solution of  
3   hydrofluoric acid.

1           12.      The method of claim 1, further comprising:

2 covering the surface regions which are not to be oxidized with a masking layer  
3 before roughening the surface of the at least one silicon surface region.

1 13. The method of claim 12, wherein the masking layer includes silicon nitride.

1 14. The method of claim 1, wherein thermally oxidizing the at least one  
2 roughened silicon surface forms a silicon dioxide layer having a thickness larger than the  
3 pore depth of the pores.

1 15. The method of claim 1, wherein the silicon surface region includes  
2 monocrystalline silicon.

1 16. A method of producing a storage trench capacitor for a memory cell having  
2 an isolation collar, comprising:

3 providing a semiconductor substrate, the semiconductor substrate having a main  
4 surface;

5 providing a trench in the semiconductor substrate, the trench extending from the  
6 main surface into the semiconductor substrate, the trench having an upper and a lower  
7 portion, the trench having a curved inner surface of silicon;

8 masking the silicon surface region of the upper portion of the trench which is not to  
9 be oxidized with a masking layer;

10 and exposing the silicon surface region of the lower portion of the trench on which  
11 a silicon dioxide layer is to be formed;

12           roughening the surface of the curved silicon surface region in the lower portion of  
13   the trench to produce a layer of porous silicon, the masking layer having a material which  
14   prevents roughening of an underlying material during roughening of the curved surface;  
15           thermally oxidizing the roughened curved silicon surface region;  
16           extending the trench into the semiconductor substrate to form a bottom portion of  
17   the trench beneath the lower portion of the trench;  
18           forming a first electrode of the capacitor in the semiconductor substrate adjacent to  
19   the bottom portion of the trench;  
20           forming a dielectric layer of the capacitor in the bottom portion of the trench; and  
21           forming a second electrode of the capacitor in the bottom portion of the trench.

1           17.    The method of claim 16, wherein the masking layer includes silicon nitride.

1           18.    The method of claim 16, wherein roughening the surface of the curved  
2   silicon surface region includes etching the surface region.

1           19.    The method of claim 16, wherein roughening the surface of the curved  
2   silicon surface region includes producing pores in the surface region, the pores having a  
3   diameter of less than 20 nm.

1           20.    The method of claims 16, wherein thermally oxidizing the at least one  
2   roughened silicon surface forms a silicon dioxide layer having a thickness larger than the  
3   depth of the pores.

1           21.    A method of producing a storage trench capacitor for a memory cell having  
2    an isolation collar, comprising:

3           providing a semiconductor substrate, the semiconductor substrate having a main  
4    surface;

5           providing a trench in the semiconductor substrate, the trench extending from the  
6    main surface, the trench having an upper portion, a lower portion, and a bottom portion,  
7    the upper portion being disposed above the lower portion which is disposed above the  
8    bottom portion, and wherein the trench having a curved inner surface of silicon;

9           forming a first electrode of the capacitor in the semiconductor substrate adjacent  
10   to the bottom portion of the trench, forming a dielectric layer in the bottom portion of the  
11   trench and forming a second electrode of the capacitor in the bottom portion of the trench;

12          masking the silicon surface region of the upper portion of the trench which is not  
13   to be oxidized with a masking layer;

14          exposing the silicon surface portion in the lower portion of the trench on which the  
15   silicon dioxide layer is to be formed;

16          roughening the surface of the curved silicon surface region in the lower portion of  
17   the trench to produce a layer of porous silicon, the masking layer having a material which  
18   prevents roughening of an underlying material during roughening of the curved surface;

19   and

20          thermally oxidizing the roughened curved silicon surface region.

1           22.    The method of claim 21, wherein the masking layer includes silicon  
2    nitride.

1           23.     The method of claim 21, wherein roughening the surface of the curved  
2     silicon surface region includes etching the surface region.

1           24.     The method of claim 21, wherein roughening the surface of the curved  
2     silicon surface region includes producing pores in the surface region, the pores having a  
3     diameter of less than 20 nm.

1           25.     The method of claim 21, wherein thermally oxidizing the at least one  
2     roughened silicon surface forms a silicon dioxide layer having a thickness larger than the  
3     depth of the pores.

1           26.     The method of claim 1, wherein the silicon surface region includes  
2     polycrystalline silicon.